period of time. Thus, the relative dielectric constant of the semiconductor device 109 can be maintained at a low level, which indicates a good state.

That is, according to the present embodiment, the wiring capacity of the semiconductor device 109 is reduced so that a product between a wiring resistance and an inter-wire capacity can be reduced. In this manner, the operating speed of a semiconductor device 109 and those of various semiconductor device using the semiconductor device 109 can be improved more significantly.

In addition, when a semiconductor device having a plurality of wiring layers laminated thereon is desired, layers such as, barrier metal 103, Cu wire 104, silicon nitride film 105, or interlayer insulation film 106 may be formed repeatedly on the first semiconductor substrate 108 via base insulation film 102 in a manner similar to the previously described manner.

In this way, even if a plurality of wiring layers are formed there is almost no apprehension that electrical performance such as inter-wire capacity is degraded. Therefore, a semiconductor device with its high throughput and various semiconductor devices can be produced.

(Sixth Embodiment)

Next, the method of manufacturing a semiconductor

device according to a sixth embodiment of the present invention is explained. FIGS. 5A - 5C show cross sectional views of a manufacturing process of a semiconductor device according to the present embodiment. The present embodiment is difference from the fifth embodiment in that a polymethyl siloxane film is used as a base insulation film 102.

First, as shown in FIG. 5A, the base insulation film 102 is formed on a surface of a semiconductor substrate 101. Here, a polymethyl siloxane film is used as the base insulation film 102.

Hereinafter, the steps of forming this polymethyl siloxane film will be described by dividing them into the steps 1 to 4.

Step 1:

A liquid-like raw material called a vanish (not shown) obtained by dissolving a film material or a polymethyl siloxane for a precursor of the film material is supplied on the surface of the silicon substrate 101. The way of supplying the vanish is the same as the step 1 of the fifth embodiment.

Step 2:

The semiconductor substrate 1, as shown in FIG. 5A, is placed on a hot plate 107 at a posture at which a surface having the vanish applied thereon is oriented upwardly. Then, the temperature of the hot plate 107 is controlled so that the vanish temperature

is held at about 80℃, the vanish is heated together with the semiconductor substrate 1, and this state is held for about one minute. In this manner, a first heating process is applied to the vanish.

Step 3:

While the semiconductor substrate 101 is placed on the hot plate 107, the temperature of the hot plate 107 is controlled so that the vanish temperature is held at about 200℃. Then, the vanish is heated together with the semiconductor substrate 101, and this state is held at about one minute. In this manner, a second heating process is applied to the vanish.

Step 4:

While the semiconductor substrate 101 is placed on the hot plate 107, the temperature of the hot plate 107 is controlled so that the vanish temperature is held at about 200℃. Then, the vanish is heated together with the semiconductor substrate 101, and this state is held at about 30 minutes. In this manner, a third heating process is applied to the vanish.

The solvent contained in the vanish applied on the semiconductor substrate 1 in the step 1 is evaporated (vaporized) and eliminated in accordance with the heating process of the steps 2 to 4 described above. In this manner, the vanish (applied film) is fixed on the semiconductor substrate 1.

After the steps 1 to 4 described above, as in the